i3 Electronics:

High Performance Packaging for Wire Bond Die

i3's organic wire bond plastic ball grid array (PBGA) carriers bring leading edge quality to system-in-package (SiP) or single chip module (SCM) precision packaging for semiconductor technology.

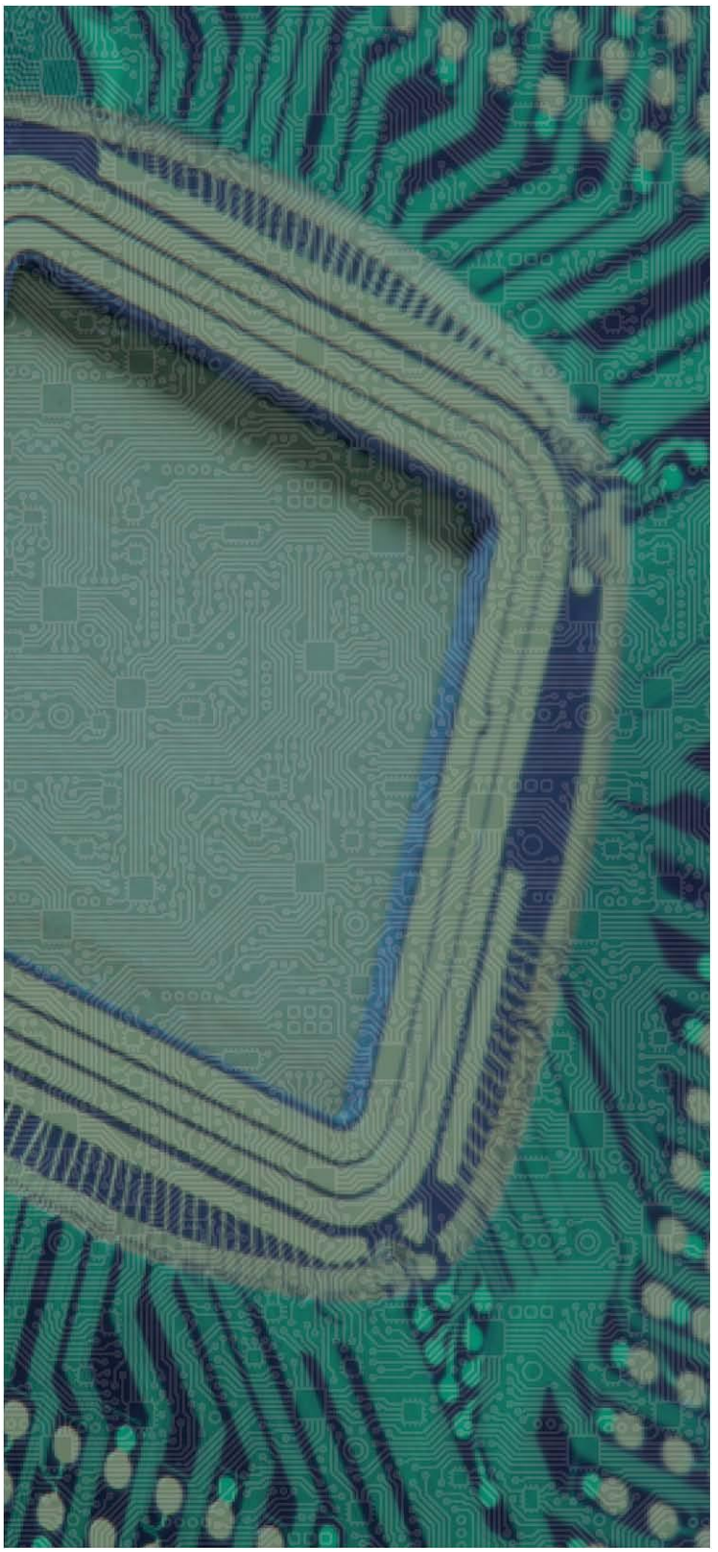
Superior electrical performance combined with materials that are matched to the printed circuit board allow wire bond PBGA carriers to deliver high overall performance and field reliability.

You can extend the use of your existing wire bond infrastructure with our PBGA carriers, available in both chip up and cavity configurations:

- The chip up design is extremely economical and targets lower power applications
- The cavity package allows the backside of a die to be thermally connected to a heat spreader. This configuration is mounted to a printed circuit board with the heat spreader exposed, allowing easy attachment of a heat sink and providing excellent thermal performance

FEATURES

- Bondfinger pitches of 118 µm enable shorter wire lengths, die shrinkage or higher I/O density
- Shorter wire bond wires, lower loop heights and increased voltage/ground connections mean significantly reduced electrical parasitics of an assembled module
- Provides the ability to migrate from a chip up package to a same size cavity package as chip power requires
- Single part number substrates can accommodate a greater chip part number mix, providing increased I/O capability
- Pick and place compatible for automated assembly
- Standard JEDEC body sizes and testing are available as well as custom sizes
- Single tier cavity leads to improved electrical performance and promotes a lower profile package
- Single layer or multi layer cross sections allows design flexibility to accommodate density needs
- Cavity package provides added thermal performance



Specifications

PERFORMANCE

Die interconnect	Wire bond, 60 um inline, 43 um staggered
Card interconnect	BGA available down to 1 mm full grid array
Package I/O count	Greater than 700
Standard compliance	JEDEC Class 3
Body size	JEDEC standard

MATERIALS

Conductor Copper

Dielectric BT, polyimide, FR4

MECHANICAL

Substrate thickness 1.00 mm

Typical PTH diameter 0.25 mm

Bond finger pitch 118 µm, no lines between pads; 194 µm, one line between pads; (97 um effective pitch)

BGA 1.00 mm, 1.27 mm

ELECTRICAL

Impedance Zo 60-100 Ohms (with ground plane) 120-150 Ohms (no power planes)

Line resistance 1.0-1.5 Ohms/cm

Propagation delay 65-70 ps/cm