CoreEZ®

i3 Electronics:
Thin Core Flip Chip Technology

Our CoreEZ® semiconductor package uses the HyperBGA® manufacturing platform to offer a thin core build up flip chip package with very dense core vias using a cost sensitive material set. The core via density provides 199 micron via to via core pitch, resulting in an essentially coreless structure.

High core via density is achieved using smaller pads and the same 50 micron laser drilled holes used in producing HyperBGA® to unblock wiring channels through the core. This enables CoreEZ® to provide up to twice the number of signal layers as a standard build up package that uses mechanically drilled core vias with large capture pads.

The end result is an extremely cost effective solution that allows full strip line signal layers on both sides of the core. Component cost is further reduced by enabling die shrink through die pad pitch reduction down to 150 microns.

In addition, the thinness of the core provides improved power distribution and the ability to dissipate chip thermal power into the PCB.

CoreEZ® is an excellent choice for applications requiring low cost build up materials along with high reliability, performance and wireability. It is also well suited to aerospace applications requiring radiation tolerance.

FEATURES

DENSITY

- 199 µm core via pitch, 50 µm laser drilled vias and 25 µm LW/LS allows full signal wiring on both sides of the core

ELECTRICAL PERFORMANCE

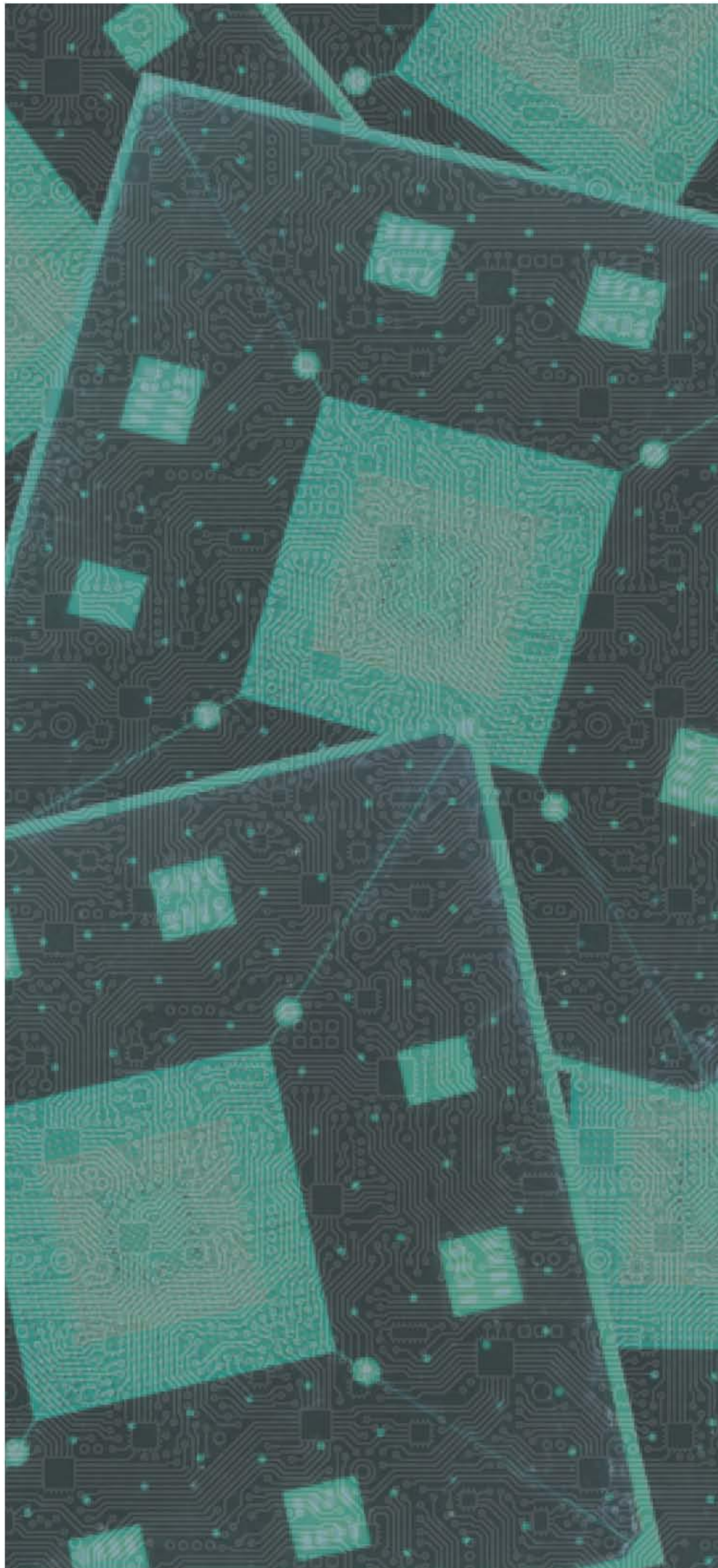
- Thin core (200 µm) build up structure reduces inductance, providing better power distribution
- High speed differential pair designs reduces electrical noise
- Up to 4 full strip line signal layers provides excellent electrical performance

RELIABILITY

- Twice the board level reliability of a standard FC PBGA or FC ceramic BGA

FLEXIBILITY

- Customizable wireability and flexibility provided with 6, 8, 10 or 12 layers
- Excellent performance with a low cost material set means no compromising
- Parts available in any shape, enabling the merger of dense circuitization found in chip packaging with configuration variety found in traditional PC board technology



Results may vary with different die, assembly processing or design attributes.

Test results for a 42.5 mm body size with a 17.3 mm die and 200 μm die pad pitch with low melt bumps and a 42.5 mm body size with a 14.7 mm die and 225 μm die pad pitch with high melt bumps.

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Specifications

Laminate

Line width	25 µm minimum
Line space	25 µm minimum
Pad diameter	100 µm minimum
Via diameter	250 µm minimum (UV laser drilled)
Minimum die pad pitch	150 µm
Build-up dielectric thickness	35 µm, 50 µm

MATERIALS

All planes Copper

Dielectrics P-Aramid in core and silica-filled high Tg epoxy resin-coated copper

FCA pad metallurgy Coined solder bumps on copper, or on 200 microinches of e Ni on 4 microinches I Au on copper

Lid metallurgy/thickness Copper/1.00 mm (substrates do not include lids)

ELECTRICAL

Build-up layer dielectric constant	3.7 up to 2.5 GHz
Build-up layer loss	0.013 to 1 MHz
Core material dielectric constant	3.7 up to 2.5 GHz
Core material dielectric loss	0.018 at 1 MHz

PHYSICAL

Build-up layer dielectric constant	3.7 up to 2.5 GHz
Build-up layer loss	0.013 to 1 MHz
Core material dielectric constant	3.7 up to 2.5 GHz
Core material dielectric loss	0.018 at 1 MHz
Single chip body sizes	JEDEC up to 55.0 mm
System-in-package body size	Custom
Number of I/Os	Up to 2916 at 1.0 mm

RELIABILITY STRESS TESTING

Board level thermal cycles	Over 4,000 cycles of 0˚ to 100˚C
High-temperature storage	150˚C for 1,000 hours
Component level thermal cycles	1,000 cycles of -55˚ to 125˚C