i3 Electronics:

Increased Wiring Density and Layer Count for Both Digital and RF Designs

Our HyperBGA® fluoropolymer-based coreless semiconductor package allows your die to run at extremely high speeds. The combination of the low loss, low dielectric constant material and strip line cross sections enable signal speeds surpassing 12 Gb/s.

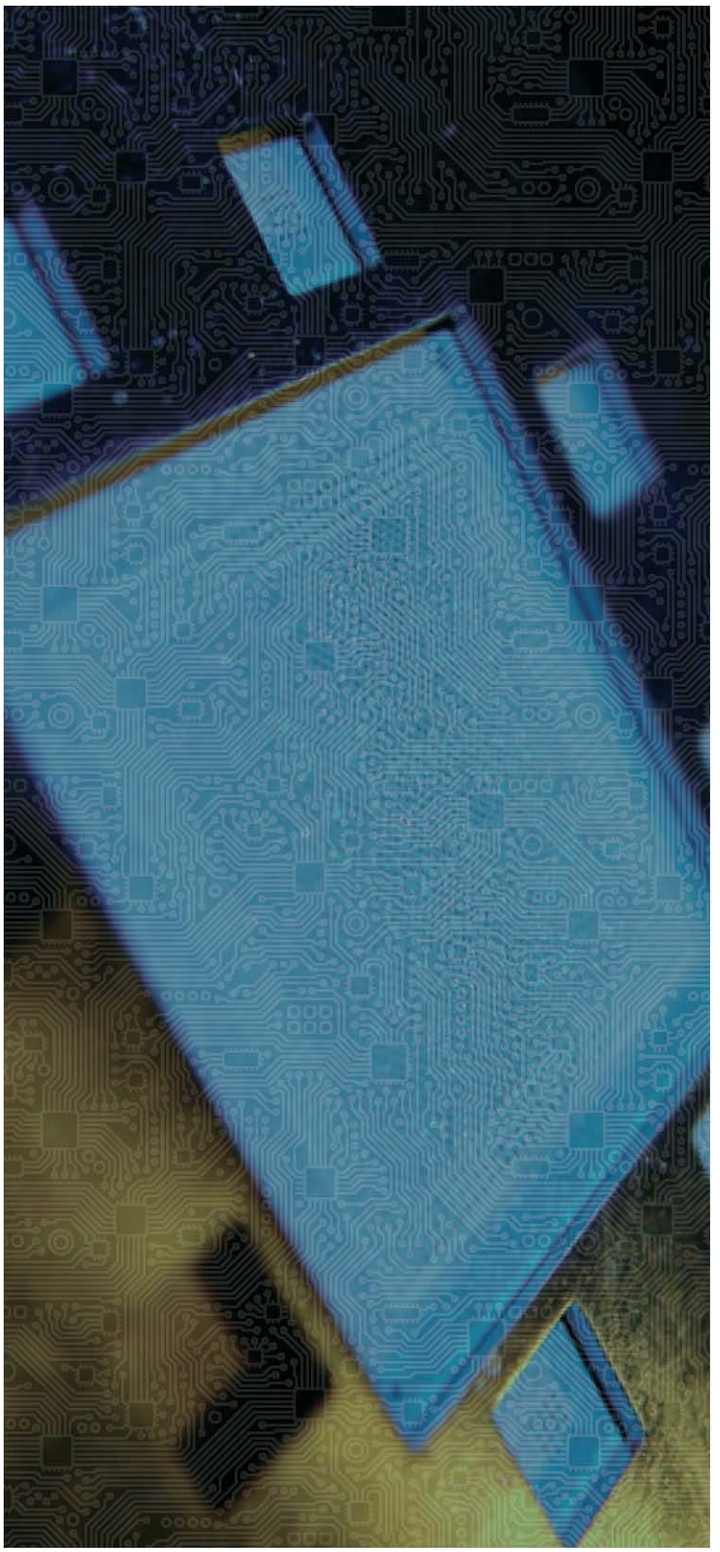
The PTFE material compliance combines with the dimensional stability of a copper-invar-copper center plane enabling HyperBGA® to provide long field life without the BGA wearout, die cracking, delamination or flip chip bump fatigue of other packages.

It's the solution for networking, high-end server, telecommunications, military and medical markets — anyplace where speed, reliability and increased signal I/O must combine with reduced size, weight and power (SWaP).

This low stress flip chip laminate package is also ideally suited to multi-layer, RF, chip-on-flex or any application requiring a system-in-package (SiP) approach.

FEATURES

- Outstanding SiP solution offers longest overall board level flip chip BGA life available
- Delivers 2-10 times the flip chip BGA package reliability over ceramic BGAs
- Assembled using standard SMT processes and materials making columns or grid array sockets unnecessary and Pb free assembly compatible
- Capable of flip chip, SMT or CSP component attach on both sides
- Compliant laminate minimizes die and BGA stress when using large die and large body sizes
- Substrate engineered to balance the CTE mismatch between silicon and printed circuit board for high reliability
- Voltage plane splits provide the ability to turn on/off a high number of selected die areas for improved power consumption and noise control
- Thin, light, low profile fits easily in tight board-to-board spaces
- Parts available in any shape, allowing the merger of dense circuitization found in chip packaging with configuration variety found in traditional PCB technology
- Domestically produced, high quality, high reliability outer dielectric ensures supply and reduces lead times
- Delivers superior performance with the combination of low loss, low dielectric constant material and strip line cross sections enabling digital signal speeds surpassing 12Gb/s
- Availability of functional module testing all under one roof



Specifications

Laminate

Line width 25 µm minimum in die area
Line space 30 µm minimum in die area
Via diameter 50 µm minimum (UV laser drilled)
Layers Up to 11

MATERIALS

Ground plane Copper-invar-copper
Outer dielectric Epoxy (PPE**)**
Flip chip metallurgy Coined 63/37 eutectic on copper or on 200 microinches of e Ni on 4 microinches I Au on copper; lead free
BGA metallurgy Presolder on copper, OSP on copper or on 200 microinches of e NI on 4 microinches I Au on copper; lead free

ELECTRICAL

Time of flight 5.6 ps/mm
Controlled impedance (Zo) 50-60 Ohms
Cross talk (Vne) <15%
Power/ground loop inductance 5-10 pH
Dielectric constant 2.7 at 1 MHz
Dielectric loss tangent 0.003 at 1 MHz

PHYSICAL

Body sizes JEDEC, 17.0 mm–55.0 mm
SiP body sizes Custom
Number of BGA I/Os Up to 2916 at 1.0 mm pitch
Die size >18.3 mm
BGA pitch 0.5 mm–1.27 mm
Decoupling capacitors Flip chip and SMT

RELIABILITY

Moisture sensitivity JEDEC Level 3
Board level thermal cycles 10,000 cycles of 0˚ to 100˚C
High-temperature storage 1,000 hours at 150˚C
Component level thermal cycles 1,000 cycles of -55˚ to 125˚C
HAST 264 hours of 110˚C/85% RH/3.7V
Pressure pot 96 hours at 121˚C/100% RH/2 ATM
Temperature, humidity, bias 1,000 hours at 85˚C/85%RH/3.7V

Results may vary with different die, assembly processing or design attributes.