PRINTED WIRING BOARD DESIGN GUIDE

Printed Wiring Board Applications Engineering
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The following are acceptable parameters as of the date of this writing. Future design variations and requirements may require a different parameter. These are for Build To Print designs.

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1.0 INTRODUCTION

This document describes the i3 Electronics (i3) printed wiring board design ground rules consistent with our capabilities and processes. Described in this document are raw card attributes which allow use of both surface mount and pin-in-hole technologies. These design ground rules are intended to provide our customers with design parameters which will result in manufacturable, low cost products. These parameters do not define the limits of our capabilities. We are producing boards which use Z-Interconnect technology, which have mixed metallurgy surface finishes or other unique requirements. Please contact us early in the design phase if your needs fall outside normal parameters.

1.1 Control

This document is maintained and controlled by Dept.0093, Applications Engineering, i3. Distribution is through Dept. 0076.

1.2 Usage

This document is intended for use by Product Development Engineers and Physical Designers familiar with printed circuit design. It is intended as a guideline not a list of requirements.

1.3 Dimensions and Tolerances

Dimensions given in this document are in inches unless otherwise noted. Further, all dimensions are design nominal, not finished product requirements, which would be noted in the applicable product drawings and specifications.

Throughout this document we assume the drilled hole diameter is .002” larger than the finished plated hole diameter.

1.4 Specifications

Unless otherwise directed i3 will build to IPC Class 2 specifications.

1.5 Data Format

Preferred, ODB++ (Valor, Frontline)
Second Choice, RS-274X (Ucamco)

2.0 PANEL SIZES

Listed below are the standard panel sizes used by i3 Electronics.

SIZE	ACTIVE DIMENSIONS	ACTIVE AREA
18.0” x 24.0”	16.5” x 22.5”	371 sq”
19.5” x 24.0”	18.18” x 22.54”	409 sq”
24.0” x 28.0”	21.64” x 25.50”	551 sq”
24.0” x 32.0”	22.50” x 30.50”	686 sq”

2.1 Panel Utilization

Panel utilization affects our ability to be cost efficient and is related to both the size of the PWB and the number and variety of coupons (IPC, impedance, IST/CITC, etc.) required on the panel as all must fit within the active area. Please contact us early in the design phase so we can work with you to optimize your PWB’s dimensions and obtain the best utilization possible.

![i3 electronics logo]

3.0 PLATED HOLES and VIAS

See the following tables

3.1 THROUGH, BLIND, and BURIED VIAS

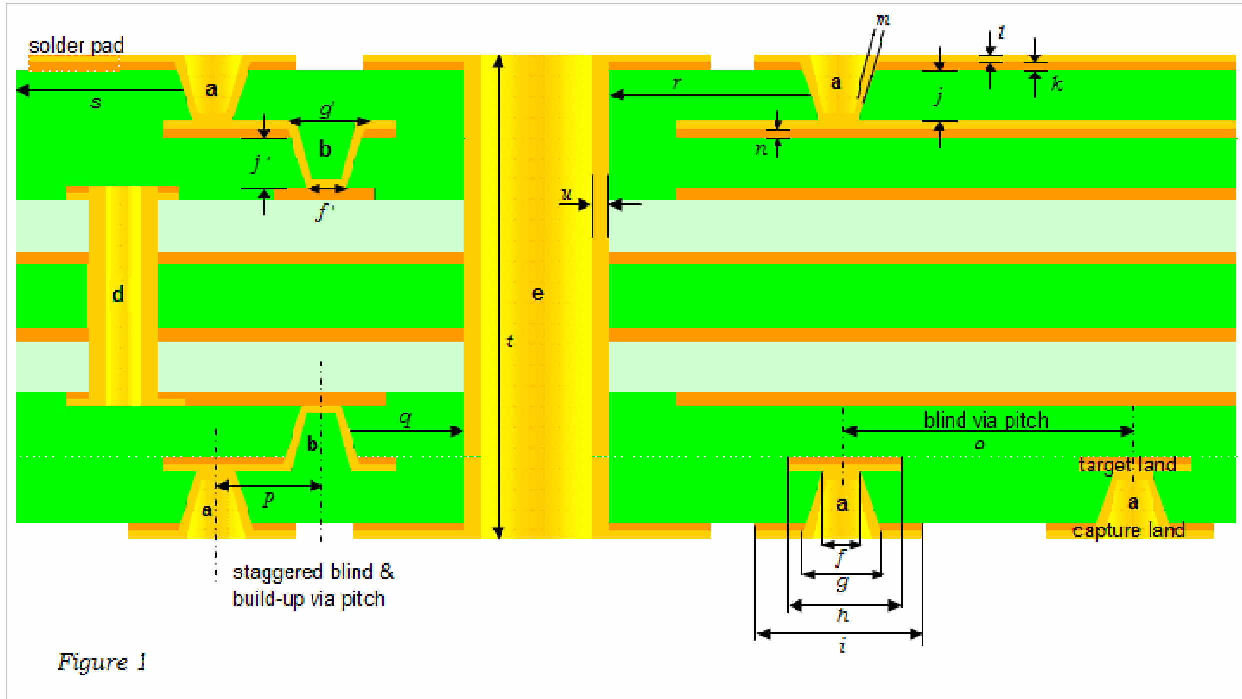


Figure 1

	Symbol	Feature	Preferred Producibility Range (in.)	Reduced Producibility Range (in.)	Comments
	a	blind microvia (build-up construction)			
	b	buried microvia (build-up construction)			
	d	subcomposite via (treated like through vias)			
	e	through via			
	f	blind uvia diameter @ target land (unplated)	.004” to .008”	.003”	
	g	blind via diameter @ capture land (unplated)	.004” to .008”	.003”	
	h	blind via target land diameter (*h=f+?*)	*h = f + .006”*	*h = f + .005”*	
	i	blind via capture land diameter (*i=g+?*)	*i = g + .006”*	*i = g + .005”*	
	j	blind via dielectric thickness (min - max)	.002” to .008”	.002” to .008”	

	blind via aspect ratio (min - max, correlate with *j*)	≤ .85/1	≤ 1/1	
k	external base Cu foil thickness	.00028” (7 microns)	.0002” (5 microns)	
l	external plated Cu thickness	.0019”	.0014”	
	external trace width	.004” min	.004” min	avoid impedance control
	external space w/o microvias	.004” min min	< .004” min	
	external space with microvias	.005” min min	< .005”	because of thicker copper
	internal trace width	.003” min	.0025”	for 0.5 ounce copper
	internal space	.004” min	< .004”	for 0 5 ounce copper
m	blind via plated Cu wall thickness	.0005” minimum	copper via fill	
n	target land Cu foil thickness (preferred, correlate with *j*)	≥.0067” (17 microns)	≥.0047” (12 microns)	total copper thickness
j'	maximum buried build-up via dielectric thickness	002” to .008”	002” to .008”	
o	minimum blind via pitch	.015”	.012”	
	blind via dia. (*f*) assumption for *o*	.004”	.003”	
p	minimum staggered blind & buried build-up via pitch (**a**-**b**)	.010”	0 (stacked)	stacked requires buried via fill + cap plate
	blind via dia.(*f*) assumption for *p*	.004”	.003”	
	buried build-up via diameter (*f '*) assumption for *p*	.004”	.003”	
q	minimum proximity, buried build-up via - through via (**b**-**e**)	.008”	.007”	
r	minimum proximity, blind via - through via (**a**-**e**)	.014”	.013”	
s	minimum proximity, blind via - PCB edge	(land dia / 2) + 50 mils	(land dia / 2) + 30 mils	
t	overall PCB thickness	not blind/buried via limited	not blind/buried via limited	through via aspect ratio limited
u	Through and subcomposite via plated Cu wall thickness	.0007”	.001”	
v	through and subcomposite via aspect ratio	≤ 14/1	≤ 20/1	
	through and subcomposite via external land diameter	Via diameter + .014” (.006” budget)	Via diameter + .012” (.005” budget)	Drill to land tangency
	through and subcomposite via internal land diameter	Via diameter +.014” (.006” budget)	Via diameter + .012” (.005” budget)	Drill to land tangency
	through and subcomposite via antipad	Via diameter + .020” (.006” budget)	Via diameter + .018” (.005” budget)	3 mil min spacing

3.2 Buried Core Vias

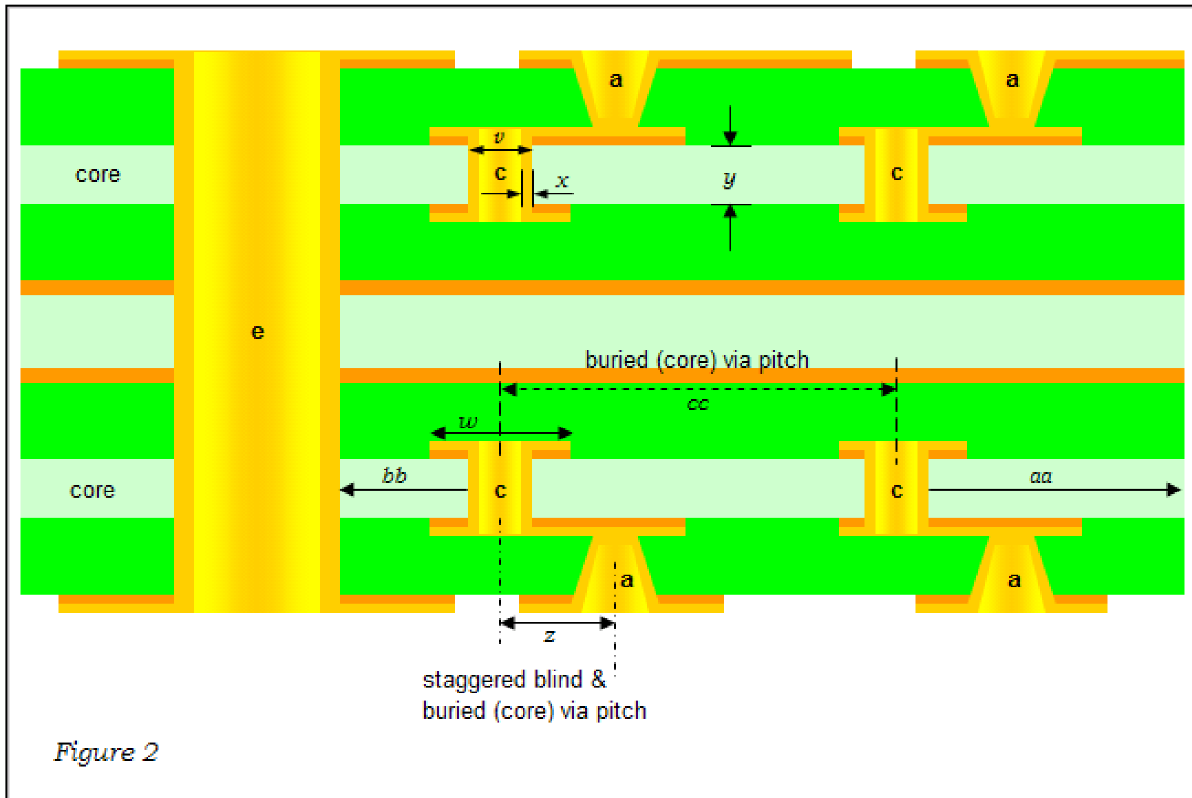


Figure 2

Symbol	Feature	Preferred Producibility Range (in.)	Reduced Producibility Range (in.)	Comments
a	blind via (build-up construction)			
b	buried via (build-up construction)			
c	buried core via (not build-up construction)			
d	subcomposite via			
e	through via			
v	buried core via diameter, unplated	.008" (mechanical)	.004" (laser)	
w	buried core via land diameter ($w = v+?$)	$w = v + .010"$	$w = v + .005"$	
	manufacturing variability for w (+/- tolerance)	+/- .001"	+/- .0005"	will vary based on copper thickness
x	buried core via Cu plating wall thickness	.0005"	.0005"	
y	buried core via dielectric thickness (min - max)	.0034" and greater	.002" to .008"	
	buried core via aspect ratio (min - max, correlate with y)	up to 10/1	up to 12/1	would consider higher aspect ratio designs
z	minimum staggered blind & buried core via pitch (**a-c**)	.010"	0 (Filled and stacked)	
	blind via diameter (f) assumption	.004"	.004"	

		for z			
		buried core via diameter (v) assumption for z	.008”	.004”	
	aa	minimum proximity, buried core via - PCB edge	(land dia / 2) + .050”	(land dia / 2) + .030”	based on power plane to edge clearance
	bb	minimum proximity, buried core via - through via	.010”	.0075”	
	cc	minimum buried core via pitch	.023”	.014”	
		buried core via diameter (v) assumption for cc	.008”	.004”	

3.3 Aspect Ratio

Drill aspect ratio is the ratio of PWB thickness to PTH drill bit diameter. For example, if a .010” drill bit is used on a .100” thick PWB the drill aspect ratio is 100/10 or 10/1 expressed as 10 to 1. i3 is capable of handling drill and plate aspect ratios up to and greater than 20 to 1.

3.4 Blind Vias / Microvias

Normally blind vias are mechanically drilled if the drill diameter is greater than .006” while microvias are laser drilled if the drill diameter is .006” or less. If the blind vias are produced by controlled depth mechanical drilling, the first power plane below target plane may require a clearance land (antipad) at the blind via location to allow for the drill bit depth control tolerance of +/- .002”. This must be considered for each stackup design.

To facilitate copper plating the aspect ratio of such holes must be less than or equal to 0.85 to 1.0 depth to diameter.

3.5 Minimizing Cost

Use industry standard drill bit sizes for non plated holes.
Maximize hole size.
Minimize number of different hole sizes.
Avoid blind or buried vias if possible.
Minimize drill and plate aspect ratio
Maximize tolerances

4.0 DESIGN FEATURES and RECOMMENDATIONS

The following are examples of various PWB features that are available to the designer. However, it is not intended as a complete list of what we offer. The i3 team will work with you to meet your unique requirements. (*i3 will not design a PWB w/ a footprint that does not match the manufacturers recommended component footprint.)

4.1 Pads Outer (Mounting Planes)

A pads outer design is one in which the two external planes have lands and SMT pads only. No wiring other than pad to the nearest via.

Advantages

a) Cost is less than wired external planes
b) Failures associated with neckdowns are reduced
c) Better radiated noise control
d) Better impedance control
e) Can plate more Cu in the hole

Disadvantages

a) Card thickness may increase because of possible need for additional signal layers for wiring
b) Loose ability to rework surface traces

4.2 Signal Trace to Edge of PWB

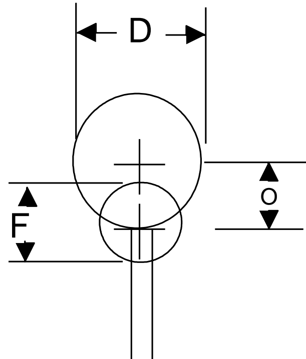
The minimum distance from a signal trace to the edge of the card should be .020”.

4.3 Nonfunctional Lands/Pads

i3 will remove nonfunctional (unused) internal signal lands/pads unless otherwise directed.

4.4 Line Entry Flares (Tear drops)

When breakout is allowed, i3 will add signal line entry flares to prevent the occurrence of damaged or severed line entries during drilling. The following diagram illustrates flares i3 will add at trace to pad entry:



The following describes how to calculate the correct flare size and location:

D = Pad Diameter
F = Flare Diameter
O = Flare Offset = Distance From Center of Pad to Center of Flare

F = Drill size + .002” (Minimum)
O (for soldered PTH) = (Trace to Pad space – .002”) + ((D-F)/2) + .0015” (minimum)
O (for compliant pin PTH) = (Trace to Pad space – .004”) + ((D-F)/2) + .0015” (minimum)

4.5 Split Power Planes

Power planes can be split for a multivoltage requirement. When doing so, a .020” wide voltage divider design is recommended. Minimum voltage divider design width is .014”.

4.6 Copper Thickness

It’s acceptable to mix ½ oz and 1 oz copper on the same core, or 1 oz and 2 oz copper on the same core. Cores with ½ oz and 2 oz copper should be avoided because of a tendency of the core to curl up excessively during manufacturing.

i3 is internally qualified to build PWBs containing copper layers up to 6.0 oz

4.7 Layup Construction

i3 can support various layup construction types including core to composite, subcomposite, and microvia designs.

4.8 Buried Resistance

Buried resistance technology can be provided through the use of industry standard materials at 10, 25, 50, 100 and 250 ohms per square. Resistor tolerance of +/-20% (+/-15% reduced producibility), as formed, when properly designed. A tolerance of <5% can be achieved with laser trim.

4.9 Non Plated Holes

Specify standard industry drill bit diameters when possible. Preferred minimum diametric tolerance is +/- .0015. A +/-.001" tolerance is manufacturable but adds to the cost.
Minimum recommended design spacings follow:
Nonplated hole to power plane, .012"
Nonplated hole to circuit line, .010"
Nonplated hole to adjacent land or other copper feature, .015"
Nonplated hole to edge of soldermask opening, .005"

4.10 Backdrilling

Backdrilling removes the unused portion of a PTH or subcomposite via barrel. It can be done from either side of a PWB or subcomposite. The typical backdrill diameter is .008" larger than the drill bit diameter used to create the original hole. The backdrill diameter needs to be considered when designing the PWB. Typical backdrill depth control capability is +/-.006" although a larger tolerance should be specified if allowed by the design. Tighter tolerances may be achieved, please contact i3 with specific requirements.

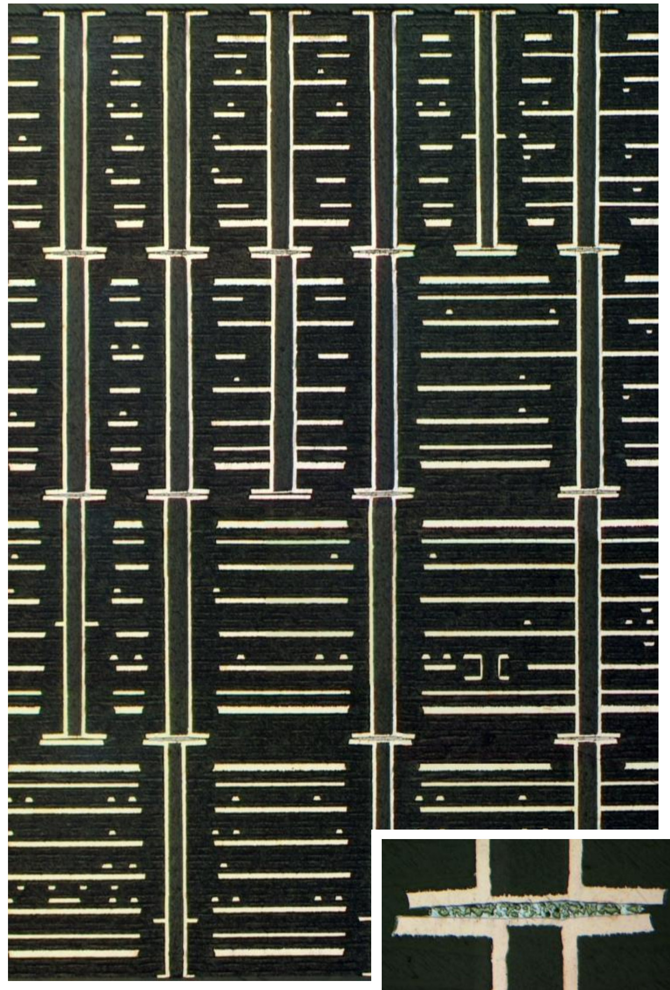
Backdrilled hole locations are typically identified by using a slightly larger PTH diameter than non backdrilled PTHs of the same size. For instance, if some .012" finished PTHs are to be backdrilled they can be identified by making them .01201" PTHs. If another group of .012" PTHs are to be backdrilled to a different depth or from a different side they can be identified as .01202" PTHs and so on. The details of each group of backdrilled PTHs, including the identification of the starting side and the do not pierce layer should be defined within the FAB drawing. Some physical design systems include backdrill definition capability. When possible, please include backdrill data files as part of fabrication package.

5.0 SUB-COMPOSITE Z-INTERCONNECT

Sub-composite Z-Interconnect technology is where conductive adhesive is used to electrically interconnect multiple sub-composites together. A designer may find this technology useful for several reasons:

- Reduced via stub length
- Increased wireability – wiring channels opened up beneath terminated vias
- Double sided, back to back component mounting
- Circuit density is so great that the circuit board is not manufacturable by conventional PTH technology
- An alternative to back drilling without the back drill wireability implications
- Mixed dielectrics – can create a “high speed” sub with exotic dielectric material and a “lower speed or power” sub with lower cost dielectric materials, without having to consider drill and plate of different dielectrics
- Other unique requirements such as ledges, steps, functional islands and others

In this technology, each sub-composite is designed using any or all of the attributes in i3’s standard Printed Wiring Board Design Guide.



5.1 Sub Z-Interconnect Capabilities

Attribute	Std Practice	Min (Max) Capability	Development
Number of sub-comps	2-4	Unlimited	Unlimited
Sub-Comp Thickness	0.020” – 0.120”	0.015” – 0.120”+	0.015” – 0.120”+
Joining Pitch (2 joined pads)	1mm	0.8mm	0.5mm (*1)
Composite Thickness (Max)	0.400”	0.500”	>0.500”
Comp. Thickness Max (w/ PTH’s)	0.250”	0.250”	>0.250” *(2)
Sub-Comp Dielectrics	Megtron 6, N4000-13, Driclad, Driclad HP	On demand	On demand
Joining Dielectric	Megtron 6, Driclad, Driclad HP	Megtron 6, Driclad, Driclad HP	On demand

(*1) Joining pitches less than 0.8mm will require different joining layer designs than those defined in this guide. Please consult with i3 prior to beginning this design.
(*2) Composite thickness >0.250” is limited by process equipment capability. If PTH’s for PIH components (e.g. compliant pin connectors) can be contained within a sub-composite, then the 0.250” thickness limitation is removed.

5.2 Joining Layer Design

The sub-composite Z-Interconnect technology requires the addition of a pads only joining layer at each sub side to be joined. For example, the top sub-composite requires a joining layer be added to the bottom, a middle sub-composite requires a joining layer on each side, while the bottom sub requires a joining layer on the top surface. The joining layer will be void of any features, except those used for joining, as defined below. Opposing joining layers will have nearly identical designs.

Joining layer design can be broken into three basic configurations:

1) Vias in both opposing subs to be electrically joined
2) A via in one sub, but not the opposing sub
3) Vias in both opposing subs, but not to be electrically interconnected

Joining layer pad stacks:

Attribute	Configuration 1	Configuration 2	Configuration 3
Sub drill diameter	0.006”-0.010”	0.006”-0.010”	0.006”-0.010”
Joining Pad Pitch (Minimum)	0.8mm	0.8mm	0.8mm
Joining Layer Pad Diameter – both subs (0.8mm pitch)	0.020”	D+0.008”	0.001”

Joining Layer Pad Diameter – both subs (1.0mm pitch)	0.026”	D+0.008”	0.001”
Joining Layer Pad Diameter for high power – (e.g. Power Bus connections)	0.040”	NA	NA
Joining Layer Pad to Pad Space (Min)	0.011”	0.011”	0.011”

Joining layer pad stack notes:

1) For joining layer pad pitches other than 0.8 and 1.0mm, use the pad diameter that is most prevalent in the design.
2) For Z-Interconnect technology, all of the sub-composite vias are drilled, plated, hole filled and cap plated. The 0.001” diameter pad defined for configuration 3 will result in complete etch off of the pad, however, the hole fill will limit etch out of the barrel plating to a depth of approximately 0.0005” from the surface. This structure has been demonstrated with thermal cycle and field use.
3) The feature dimensions for configuration 3 can be used for configuration 2 structures, if desired. The result will be reduced risk of shorting.

5.3 Cost and Manufacturability Considerations

In order to achieve the lowest cost, it is desired that sub-composites can be fully processed and tested, with the exception of soldermask and surface finish, and thus they can be joined, surface finished, electrically tested and shipped. However, designs can include composite PTH’s, if required, as long as overall composite thickness is equal to or less than 0.250”. The requirement for PTH processing can impact yield, as well as, limit testability of the sub-composites. Alternatively, i3 has fabricated Z-Interconnect boards with “blind” compliant pin connector holes (see Figure 1) and with PIH connector holes in 1 sub only, at a Z-Interconnect formed ledge (see Figure 2).

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To aid manufacturability, it is desired that each sub-composite be symmetrical within itself. To minimize board warpage, it is desired that the overall composite stack-up be symmetrical. It is not necessary for the different sub stack-ups to be identical to each other.

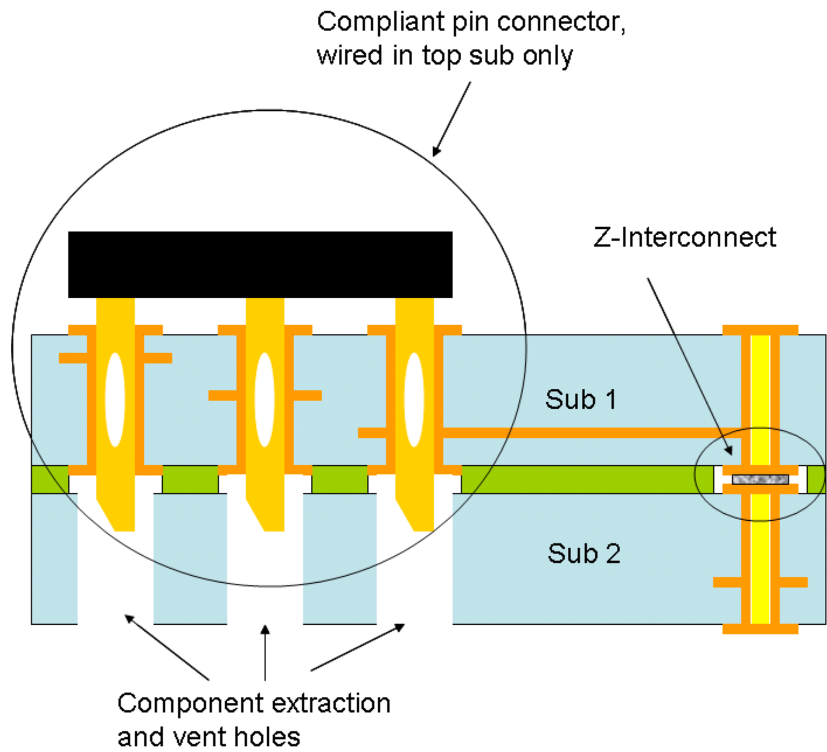


Figure 1: Compliant Pin Connector Option with Z-Interconnect

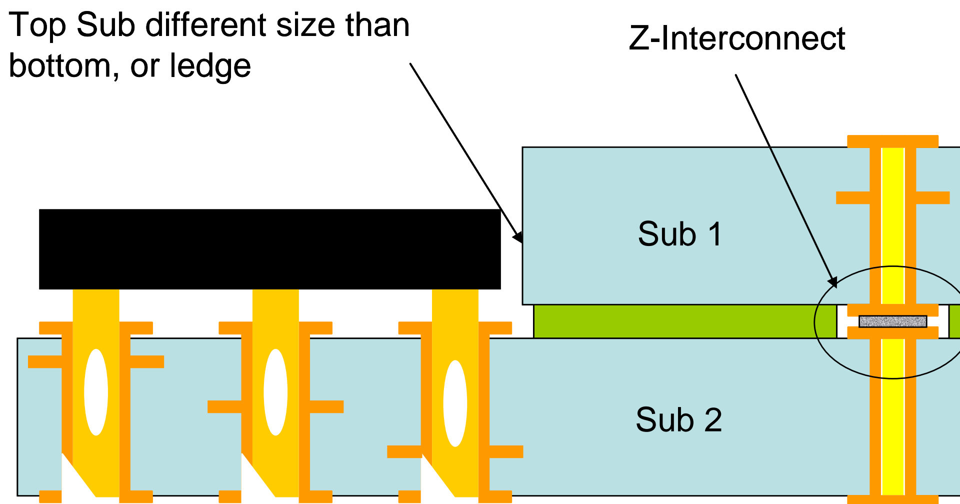


Figure 2: Different size subs, ledges, cavity options with Z-Interconnect

6.0 SOLDERMASK and VIA FILL/PLUG

6.1 Plugged Vias

A plugged via is a via which is intended to be partially filled with solder mask. Holes are typically plugged from one side only and are normally NiAu or HASL plated prior to plugging to protect the PTH from process related corrosion.

6.2 Tented Vias

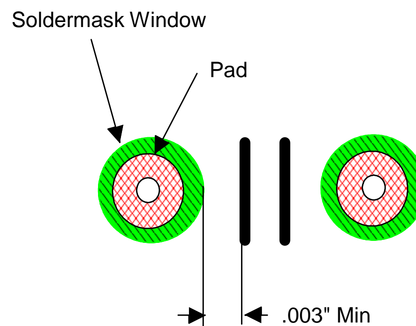
A tented via is a via which does not have a solder mask window around it, thus allowing the solder mask to cover the via. Vias are often tented under “components” to prevent the paste flux from running into the holes and onto the opposite side of the card, or to allow vacuum hold down on test equipment. Tenting is often done on both sides of the PWB. Tenting is normally done with a dry film solder mask rather than a liquid photoimagable solder mask.

6.3 Filled Vias

A filled via is intentionally filled with solder mask or other non-conductive or conductive fill material. i3 has the capability of using both industry standard and i3 unique materials.

6.4 Circuit Trace Overlap

Circuit Trace Overlap is defined as the distance from the edge of the solder mask window to the edge of the nearest circuit trace. The minimum recommended design overlap spacing is .003”.



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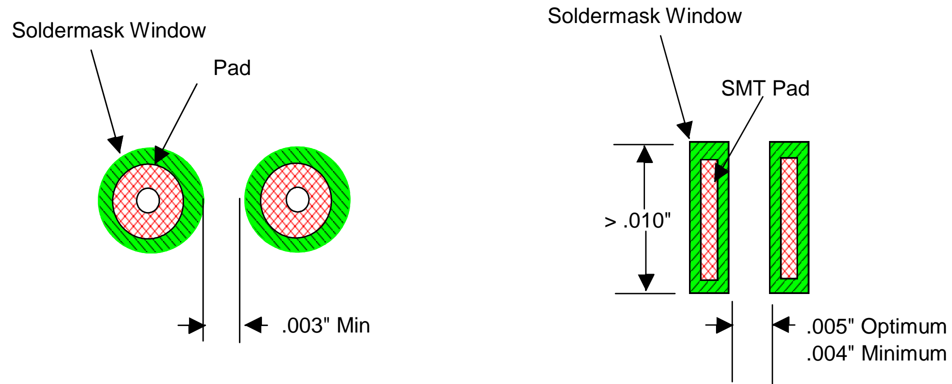
6.5 Solder Dam

A solder dam is defined as the distance from the edge of one solder mask window, to the edge of an adjacent solder mask window.

When the Dam length is > .010", the optimum dam width is .005". The minimum recommended dam width is .004"
When the Dam length is ≤ .010", the minimum recommended dam width is .003".



7.0 SURFACE FINISHES

i3 has several surface finishes available including the following. Surface finish combinations are also possible. Contact us if you have such a requirement.

Type	Comment
OSPs	Entek CU 56, Glicoat F2LX
HASL	Hot Air Solder Level, 50 to 1000 microinch
SnPb	Tin Lead, 300 microinch minimum
Hard Gold	Electrolytic, 30 microinch minimum typical
ENIG	Electroless Nickel, Immersion Gold per IPC 4552
ENEPIG	Electroless Nickel, 100 microinch minimum, Electroless Palladium, 10 microinch, Immersion Gold, coverage only
IAg	Immersion Silver per IPC 4553
Soft Au	Electrolytic, wire-bondable (needs commoning)
Soft Au	Electroless, wire-bondable

8.0 SILK SCREEN

8.1 Dimensions

	Screen Print Process	**Photoimagable Ink Process**
Image to Feature Spacing	0.015" + ½ stroke width min.	0.002" minimum
Line Width (stroke)	0.006" minimum	0.004" minimum
Character Size (W x H)	0.030" x 0.030" minimum	< 0.030" x 0.030" (1)

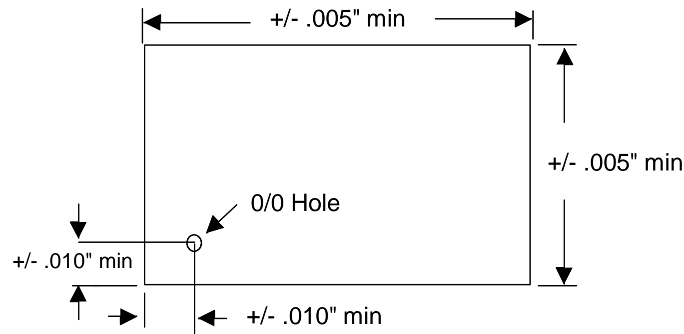
(1) Characters less than 0.030 x 0.030" are possible but may not be legible without a scope.

8.2 Restrictions

The silk screen outline should be located a minimum of 0.100" outside the component body. No silk screen features are allowed on solderable or plated surfaces.

9.0 FABRICATION DRAWING

The drawing depicting the size and shape of the PWB should show the necessary dimensions and tolerances which are required to create the PWB. The drawing below shows the minimum dimensions required on a drawing with the tightest tolerances recommended.



The attributes below are shown with the minimum acceptable manufacturable tolerances:

9.1 Minimum Location Tolerances

	Std	Special Handling
From drilled hole to profiled edge	±0 .010”	± 0.010” > x > ± 0.005”
From round artwork fiducial to profiled edge	±0.010”	± 0.010” > x > ± 0.005”
From drilled hole to drilled hole	±0.003”	

9.2 Minimum Size Tolerances

	Std	Special Handling
From profiled edge to profiled edge	± 0.005”	± 0.005” > x > ± 0.004”
On drilled holes up to 0.187” diameter	± 0.003”	± 0.003” > x > ± 0.002”
For profiled holes (> .187”)	± 0.005”	± 0.005” > x > ± 0.003”
On Radii	± 0.005”	± 0.005” > x > ± 0.003”
On the width of non-critical slots	± 0.005”	± 0.005” > x > ± 0.004”
On precision profiled slots (critical)	± 0.003”	± 0.003” > x > ± 0.002”
Hole size tolerance	±.0.003”	

9.3 In-Panel Bevel

Standard bevel angle	20°, 30°, & 45°
Depth of cut from top thru bottom	± 0.004”
Length of bevel cut	± 0.015”
Registration of bevel cut to artwork, or drilled card 0/0 hole	± 0.010”

9.4 Card Edge Bevel

	Std
Standard bevel angle	20°, 30°, 45°, & 180°
Tolerance on length of bevel cut	± 0.010”

9.5 Scoring

Sides	Double (No single sided)
Standard Score Angles	30° included angle
Tolerance on remaining web thickness	± .005”
Web thickness (nominal)	.015”
Tolerance on registration of the Score cut to an artwork feature, or drilled card 0/0 hole	± .010”

9.6 Other Requirements

The following additional information should be included on the fabrication drawing:

1. Stackup information or reference to drawing containing this information.
2. Dielectric material or material characteristics.
3. Hole sizes and counts.
4. Surface finish requirements
5. Test requirements if more than shorts and opens testing is needed.
6. Impedance requirements if any. Include trace width for single ended impedance. Include trace width and edge to edge spacing if differential impedance control required. Include impedance target and tolerance.
7. Applicable specifications.